Hi3518A Professional HD IP Camera SoC

Brief Data Sheet

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Hi3518A Professional HD IP Camera SoC

Key Specifications

Processor

- ARM926
  - Up to 440 MHz
  - 16 KB I-cache, 16 KB D-cache

Video Encoding

- H.264 baseline profile
- H.264 main profile Level 4.0
- MJPEG/JPEG baseline

Video Encoding Performance

- At most 2-megapixel resolution for H.264 encoding
- Real-time H.264&JPEG encoding of multiple types of streams: 720p@30 fps+VGA@30 fps +QVGA@30 fps+720p@1 fps JPEG snapshot
- JPEG snapshot of 720P@30 fps
- CBR, VBR, and ABR, ranging from 16 kbit/s to 20 Mbit/s
- Encoding frame rate, ranging from 1/16 frame/s to 30 frame/s
- Eight ROIs
- OSD overlay of eight regions before encoding

Intelligent Video Analysis

- Integrated intelligent analysis acceleration engine, supporting motion detection, boundary guard, and video diagnosis

Video and Graphic Processing

- 3D denoise, pre-processing, image enhancement, edge enhancement, and de-interlace
- Anti-flicker processing for output videos and graphics
- 1/16x to 8x video scaling
- 1/2x to 2x image scaling
- OSD overlay pre-processing for eight areas during encoding
- Hardware graphics overlay post-processing for the videos at two layers (video layer and graphics layer 1)

ISP

- Adjustable 3A function
- Highlight compensation, backlight compensation, gamma correction, and color enhancement
- Defect pixel correction, denoise, and digital image stabilizer
- Defogging
- Lens distortion correction
- Rotation by 90 °or 270 °
- Mirror and flip
- Digital WDR and tone mapping
- PC and ISP tuning tools

Audio Codec

- Voice codec in compliance with multiple protocols by using software
- G.711, ADPCM, and G.726 encoding
- Echo cancellation

Security Engine

- AES, DES, and 3DES encryption and decryption algorithms by using hardware
- Digital watermark

Video Interfaces

- Input
  - 8-/10-/12-bit RGB Bayer input, a maximum of 74.25 MHz clock frequency
  - BT.601
  - BT.656
  - Compatibility with mainstream CMOSs provided by SONY, Aptina, OmniVision, and Panasonic
  - Compatibility with the CCD sensor
  - Various sensor voltages
  - Programmable sensor clock output
  - At most 2-megapixel input resolution
- Output
  - 1-channel CVBS output, automatic load detection
  - One 1080p@30 fps BT.1120 VO interface for connecting to the external HDMI or SDI interface

Audio Interfaces

- Integrated audio codecx1, 16-bit voice inputs and outputs

Peripheral Interfaces

- POR
- High-accurate RTC
- A dual-channel SAR-ADC
- UARTx3
- IRx1, I^2Cx1, SPIx2 in master/slave mode, and GPIOs
- PWMx3
- SDIO 2.0x1, SDHC
- USB 2.0 hostx1
- RMII and MII modes, 10 Mbit/s or 100 Mbit/s full-duplex or half-duplex mode, providing PHY clock output

External Memory Interfaces

- DDR2 or DDR3 SDRAM
  - 16-bit DDR2/DDR3@440 MHz
  - Maximum capacity of 2Gbit
- SPI/NOR flash
  - 1-, 2-, or 4-bit SPI/NOR flash
- NAND flash
  - 8 bits
  - SLC, MLC, and 1-, 4-, 8-, or 24-bit ECC
  - Components with 8 GB capacity or larger
- NOR flash or NAND flash boot mode

SDK

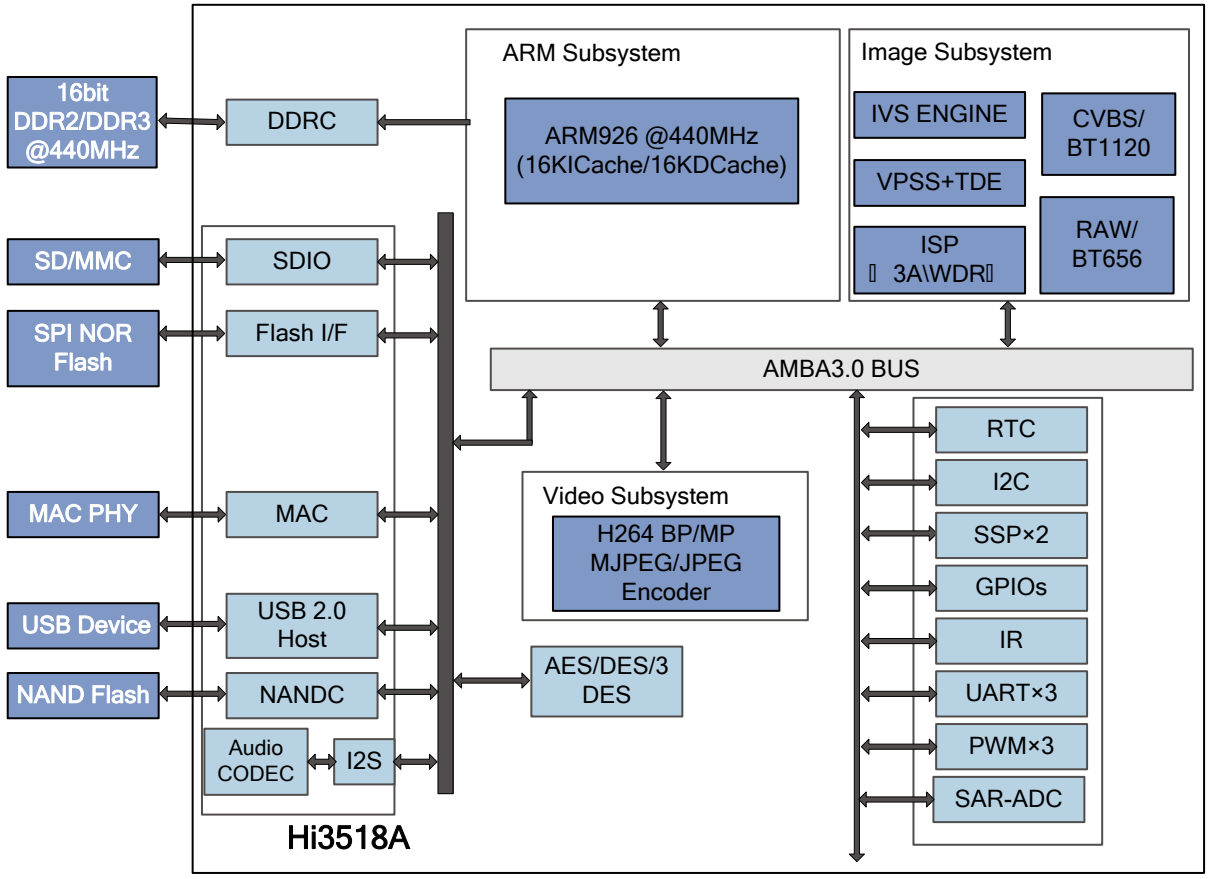
- SDK based on Linux-3.0.y
- High-performance H.264 PC decoding library

Physical Specifications

- Power consumption
  - Typical power of 700 mW
  - Multiple-level power-saving modes

- Operating voltage
  - 1.2 V core voltage
  - 3.3 V I/O voltage, and 3.8 V tolerance voltage
  - 1.5 V or 1.8 V DDR SDRAM voltage (1.5 V for DDR3 or 1.8 V for DDR2)
- Package
  - 293-pin TFBGA Package with 13 x 13 body size, 0.65 pitch

Functional Block Diagram



The Hi3518A is a new-generation SoC designed for the HD IP camera. It has a new-generation ISP and H.264 encoder. It uses an optimized pre-encoding image algorithm, advanced low-power technology, and low-power architecture. The Hi3518A features low bit rate, high picture quality, and low power consumption. The Hi3518A also supports 90 °or 270 °rotation and lens distortion correction. These innovative features enable the Hi3518A to meet requirements of different surveillance applications. It fully supports 3A algorithms, which allow customers to design different types of IP cameras including the IP AF zoom module. Because the Hi3518A integrates the POR, RTC, and audio CODEC, and supports various sensor voltages and clock outputs, the EBOM costs for the Hi3518A HD IP camera are significantly reduced. Similar to the DVR or NVR SDK, the Hi3518A SDK allows rapid mass production and facilitates system layout of IP cameras, DVRs, and NVRs.

Hi3518A HD IP Camera Solution